UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/898,068	07/05/2001	Mutsuyoshi Ito	SON-2158	1305

23353 7590 03/19/2004

RADER FISHMAN & GRAUER PLLC
LION BUILDING
1233 20TH STREET N.W., SUITE 501
WASHINGTON, DC 20036

EXAMINER	
GRAYBILL, DAVID E	
ART UNIT	PAPER NUMBER
2827	

DATE MAILED: 03/19/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/898,068	ITO, MUTSUYOSHI	
	Examiner	Art Unit	
	David E Graybill	2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *2,7-11,13 and 15-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *2,7-11,13 and 15-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 April 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☒ Other: *2 pages Decision on Petition*.

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 2, 13 and 9-11 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claims contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. The undescribed subject matter is the claims 2 and 13 limitation, "encapsulated by encapsulating resin as said semiconductor device is mounted on said mounting portion."

In the rejections infra, generally, reference labels are recited only for the first recitation of identical claim elements.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 2, 7-11, 13 and 15-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of applicant's admitted prior art and Higgins (5291062).

At page 1, line 7 to page 4, line 6; and page 6, line 3, applicant admits as prior art the following:

A semiconductor package comprising: a first insulating substrate 72 carrying a mounting portion 79 for mounting a semiconductor device and a first electrically conductive pattern 76 electrically connected 84 to said semiconductor device, a sidewall section 75 formed upright around said mounting portion of said first insulating substrate; a cavity 82 defined by said first insulating substrate and the sidewall section and encapsulated by encapsulating resin 86; through-holes 91 formed in said sidewall section, wherein solder lands 76 are provided at least in said cavity on one surface of said first insulating substrate, wherein a heat radiating plate 93 is provided on an opposite surface of said first insulating substrate; wherein said first insulating substrate is a laminated sheet lined with copper on said one surface and on said opposite surface; wherein said encapsulating resin is planarized.

A method for the preparation of a semiconductor package comprising the steps of: forming a mounting portion for mounting a semiconductor device and a first electrically conductive pattern for electrically connecting the semiconductor device on a first insulating substrate; layering a spacer having an opening of substantially the same size as said mounting portion in one surface of said first insulating substrate; mounting a semiconductor

device in said mounting portion defined by said first insulating substrate and the opening provided in said spacer; encapsulating said cavity with encapsulating resin after mounting said semiconductor device in said mounting portion; forming a through-hole for establishing electrical connection between said first electrically conductive pattern and a second electrically conductive pattern 88; and forming solder lands at least on said cavity on said electrically conductive pattern, wherein said second insulating substrate is a laminated sheet lined on one side with the second electrically conductive pattern; wherein said first insulating substrate is a laminated sheet lined on both sides of the insulating substrate with copper.

A method for the preparation of a semiconductor package comprising the steps of forming a mounting portion for mounting a semiconductor device and a first electrically conductive pattern for electrically connecting the semiconductor device on a first insulating substrate; layering a spacer having an opening of substantially the same size as said mounting portion in one surface of said first insulating substrate; mounting a semiconductor device in said mounting portion defined by said first insulating substrate and the opening provided in said spacer; encapsulating said cavity with encapsulating resin after mounting said semiconductor device in said mounting portion; forming a through-hole for establishing electrical connection between said first electrically conductive pattern and a second

electrically conductive pattern; forming solder lands at least on said cavity on said electrically conductive pattern; and providing a heat radiating plate on the opposite surface of said first insulating substrate after forming said second electrically conductive pattern; wherein said first insulating substrate is a laminated sheet lined on both sides of the insulating substrate with copper.

A semiconductor package comprising: a first insulating substrate 72 carrying a mounting portion 79 for mounting a semiconductor device and a first electrically conductive pattern 76 electrically connected 84 to said semiconductor device, a sidewall section 75 formed upright around said mounting portion of said first insulating substrate; a cavity 82 defined by said first insulating substrate and the sidewall section and encapsulated by encapsulating resin 86; through-holes 91 formed in said sidewall section, wherein solder lands 76 are provided at least in said cavity on one surface of said first insulating substrate; wherein said second insulating substrate is a laminated sheet lined on one side with the second electrically conductive pattern; wherein said encapsulating resin is planarized.

However, applicant does not appear to explicitly admit as prior art the package comprising the cavity encapsulated by encapsulating resin as said semiconductor device is mounted on said mounting portion.

Nevertheless, the product of Higgins inherently possesses the structural characteristics imparted by the process limitation, "encapsulated by encapsulating resin as said semiconductor device is mounted." See In re Fitzgerald, Sanders, and Bagheri, 205 USPQ 594 (CCPA 1980).

Also, applicant does not appear to explicitly admit as prior art a second insulating substrate provided in said cavity and on said sidewall section and carrying a second electrically conductive pattern electrically connected to said first electrically conductive pattern via through-holes; wherein said second insulating substrate includes a cavity surface and a connection surface, said cavity surface being adjacent and in contact with said cavity and said sidewall section, said connection surface being opposite said cavity surface, said connection surface having a plurality of external electrical connections thereon, an external electrical connection of said plurality of external electrical connections providing a connection to an apparatus external from said semiconductor package, some external electrical connections of said plurality of external electrical connections being opposite said cavity, and other external electrical connections of said plurality of external electrical connections being opposite said sidewall section; layering a second insulating substrate carrying a second electrically conductive pattern on one surface thereof on said spacer; forming a through-hole for establishing electrical connection between said first electrically conductive

pattern and said second electrically conductive pattern; wherein said second insulating substrate is a laminated sheet lined on one side with copper; wherein said encapsulating resin is planarized prior to said step of layering said second insulating substrate.

Nonetheless, at column 2, lines 24-27; column 5, line 27 to column 6, line 15; and column 7, line 66 to column 8, line 25, Higgins discloses a second insulating substrate 52 provided in the cavity 106 and on the sidewall section 44, 46 and carrying a second electrically conductive pattern 54 electrically connected to the first electrically conductive pattern 48; wherein the second insulating substrate includes a cavity surface and a connection surface "outer surface," the cavity surface being adjacent and in contact with the cavity and the sidewall section, the connection surface being opposite the cavity surface, the connection surface having a plurality of external electrical connections 56 thereon, an external electrical connection of the plurality of external electrical connections providing a connection to an apparatus "board" external from the semiconductor package, some external electrical connections of the plurality of external electrical connections being opposite the cavity, and other external electrical connections of the plurality of external electrical connections being opposite the sidewall section; layering a second insulating substrate carrying a second electrically conductive pattern on one surface thereof on the spacer;

establishing electrical connection between the first electrically conductive pattern and the second electrically conductive pattern; wherein the second insulating substrate is a laminated sheet lined on one side with the second electrically conductive pattern.

Moreover, it would have been obvious to combine this process and product of Higgins with the process and product of the applied prior art because, as disclosed by Higgins, it would enable an entire surface of the package to be used for input/output connections without degrading thermal management of the package.

The combination of applicant's admitted prior art and Higgins does not appear to explicitly disclose wherein the second insulating substrate is lined on one side with copper.

Regardless, as cited, Higgins teaches wherein the second insulating substrate is lined on one side with the second electrically conductive pattern, and, as cited, applicant admits that a copper electrically conductive pattern is well known. Therefore, it would have been obvious to combine the product of applicant's admitted prior art and the product of Higgins because it would provide the second electrically conductive pattern.

Also, the combination of applicant's admitted prior art and Higgins does not appear to explicitly disclose wherein said encapsulating resin is planarized prior to said step of layering said second insulating substrate.

Notwithstanding, it would have been obvious to perform the process wherein said encapsulating resin is planarized prior to said step of layering said second insulating substrate because it would enable access to the encapsulant in the open cavity to planarize the encapsulant.

In any case, it would have been an obvious matter of design choice bounded by well known manufacturing constraints and ascertainable by routine experimentation and optimization to choose the particular claimed sequence because applicant has not disclosed that the limitation is for a particular unobvious purpose, produces an unexpected result, or is otherwise critical. Moreover, it is well established that, in a well known process, the order of performing process steps is prima facie obvious in the absence of new or unexpected results. Ex parte Rubin 128 USPQ (PO BdPatApp 1959).

Applicant's remarks filed 12-19-3 have been fully considered and are adequately addressed by the rejections supra.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Any telephone inquiry of a general nature or relating to the status (MPEP 203.08) of this application or proceeding should be directed to Group 2800 Customer Service whose telephone number is 571-272-2815.

Any telephone inquiry concerning this communication or earlier communications from the examiner should be directed to David E. Graybill at (571) 272-1930. Regular office hours: Monday through Friday, 8:30 a.m. to 6:00 p.m.

The fax phone number for group 2800 is (703) 872-9306.

David E. Graybill
Primary Examiner
Art Unit 2827

D.G.
15-Mar-04